CLAIMS

1. A semiconductor memory using a DDL circuit having a dummy delay corresponding to delay between an internal clock delay and an external clock, a variable delay addition circuit having a means for adjusting delay amount by a delay amount adjusting signal, and a phase comparison circuit for comparing a phase of an internal clock with that of a delay clock inputted through the variable delay addition circuit and the dummy delay and outputting the delay amount adjusting signal to the variable delay addition circuit, the semiconductor memory comprising:

a means for inputting a first signal outputted during one clock cycle of the internal clock to the variable delay addition circuit through the dummy delay at a start of burst; and

a means for detecting duration time of an active logical value of the first signal inputted from the variable delay addition circuit through the dummy delay until one clock cycle of the internal clock is completed, and setting an initial value of the delay amount of the variable delay addition circuit based on the duration time at the start of burst.

2. A semiconductor memory using a DDL circuit having a dummy delay corresponding to delay between an internal clock delay and an external clock, a variable delay addition circuit having a means for adjusting delay amount by a delay amount adjusting signal, and a phase comparison circuit for comparing a phase of an internal clock with that of a delay clock inputted through the variable delay addition circuit and the dummy delay and outputting the delay amount adjusting signal to the variable delay addition

circuit, the semiconductor memory comprising:

a means for inputting a first signal set at a logic "1" during one clock cycle of the internal clock to the variable delay addition circuit through the dummy delay at a start of burst; and

a means for detecting duration time of the logic "1" of the first signal inputted from the variable delay addition circuit through the dummy delay until one clock cycle of the internal clock is completed, and setting an initial value of the delay amount of the variable delay addition circuit based on the duration time at the start of burst.

3. A semiconductor memory using a DDL circuit having a dummy delay corresponding to delay between an internal clock delay and an external clock, a variable delay addition circuit having a means for adjusting delay amount by a delay amount adjusting signal, and a phase comparison circuit for comparing a phase of an internal clock with that of a delay clock inputted through the variable delay addition circuit and the dummy delay and outputting the delay amount adjusting signal to the variable delay addition circuit, the semiconductor memory comprising:

a means for inputting a first signal set at a logic "1" during one clock cycle of the internal clock to the variable delay addition circuit through the dummy delay as an initialization mode at a start of burst;

a means for detecting duration time of the logic "1" of the first signal inputted from the variable delay addition circuit through the dummy delay until one clock cycle of the internal clock is completed, and setting an initial value of the delay amount of the variable delay addition circuit based on the

duration time as the initialization mode at the start of burst; and

a clock outputting means for generating an output clock that synchronizes with the external clock one clock cycle behind with the internal clock delayed by the variable delay addition circuit and with the delay amount corrected by the phase comparison circuit as a lock mode after the initial setting of the delay amount in the variable delay addition circuit.

4. The semiconductor memory according to any one of claims 1 to 3, wherein

the DLL circuit can implement a standby mode with the external clock and internal clock completely stopped when a reading operation is not performed, and output readout data in an extremely short time from the start of the reading operation.

5. The semiconductor memory according to any one of claims 1 to 3 further comprising a means for setting externally the DLL circuit to be used or not.

6. A semiconductor memory using a DDL circuit having a dummy delay corresponding to delay between an internal clock delay and an external clock, a variable delay addition circuit with a means for adjusting delay amount by a delay amount adjusting signal, and a phase comparison circuit for comparing a phase of an internal clock with that of a delay clock inputted through the variable delay addition circuit and the dummy delay and outputting the delay amount adjusting signal to the variable delay addition

circuit, the semiconductor memory comprising:

a means for inputting a first signal set at a logic "1"during one clock cycle of the internal clock to the variable delay addition circuit through the dummy delay as an initialization mode at a start of burst;

a means for detecting duration time of the logic "1" of the first signal inputted from the variable delay addition circuit through the dummy delay until one clock cycle of the internal clock is completed, and setting an initial value of the delay amount of the variable delay addition circuit based on the duration time as the initialization mode at the start of burst;

a clock outputting means for generating an output clock that synchronizes with the external clock one clock cycle behind with the internal clock delayed by the variable delay addition circuit and with the delay amount corrected by the phase comparison circuit as a lock mode after the initial setting of the delay amount in the variable delay addition circuit; and

a function to switch the DLL circuit between use and nonuse by user setting with a command decoder for decoding an address signal for specifying a user-specified command and a data signal for specifying a user-specified command, and a command register for storing the output of the command decoder as the lock mode after the initial setting of the delay amount in the variable delay addition circuit.

7. The semiconductor memory according any one of claims 1, 2, 3 or 6 further comprising a means for automatically setting a latency one clock shorter than the clock latency set by the user and making the latency when seen externally the same as that set by the user.

8. The semiconductor memory according to any one of claims 1, 2, 3 or 6 further comprising a reset means for resetting the DLL circuit at the start of burst.